

Fig. 1

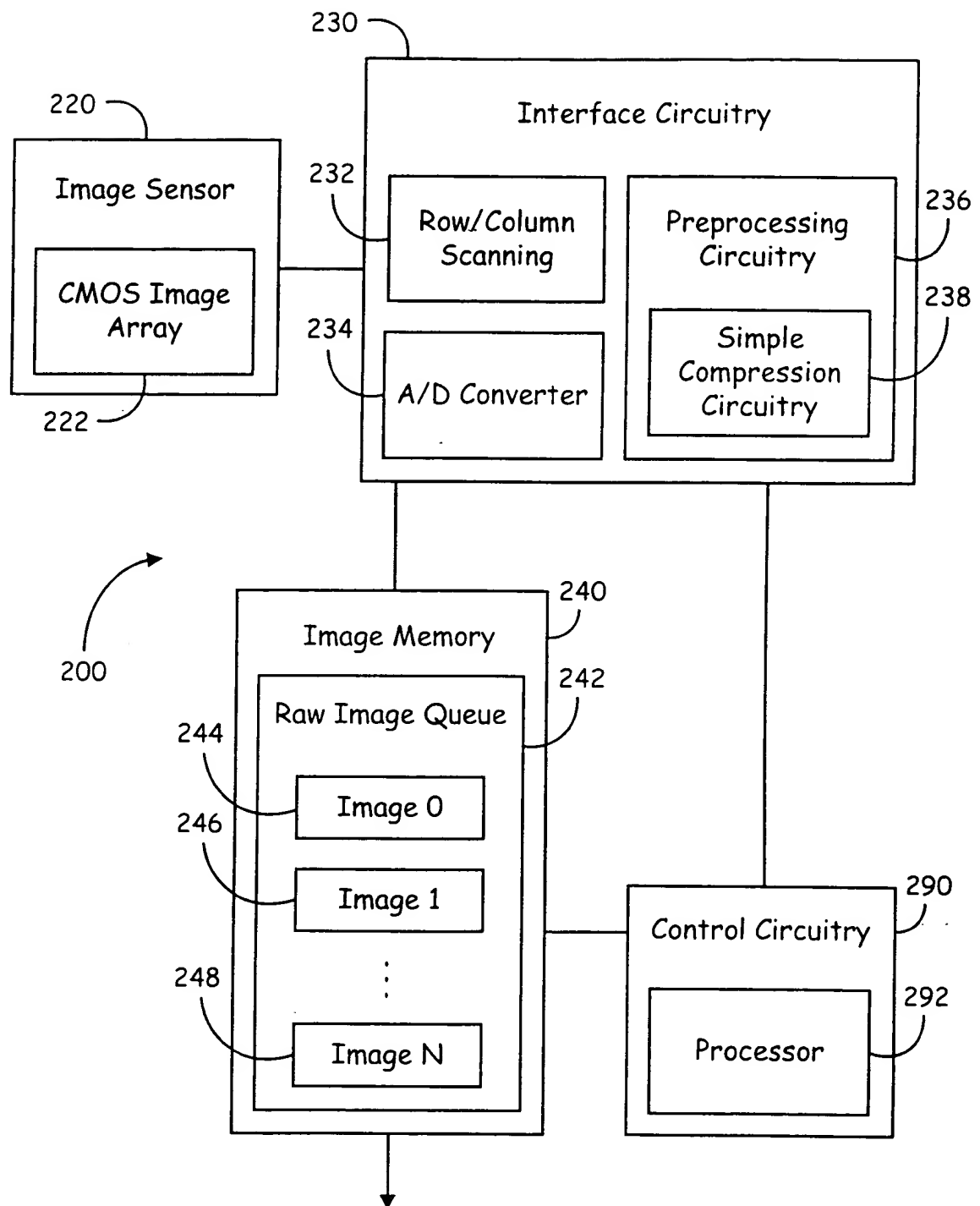


Fig. 2

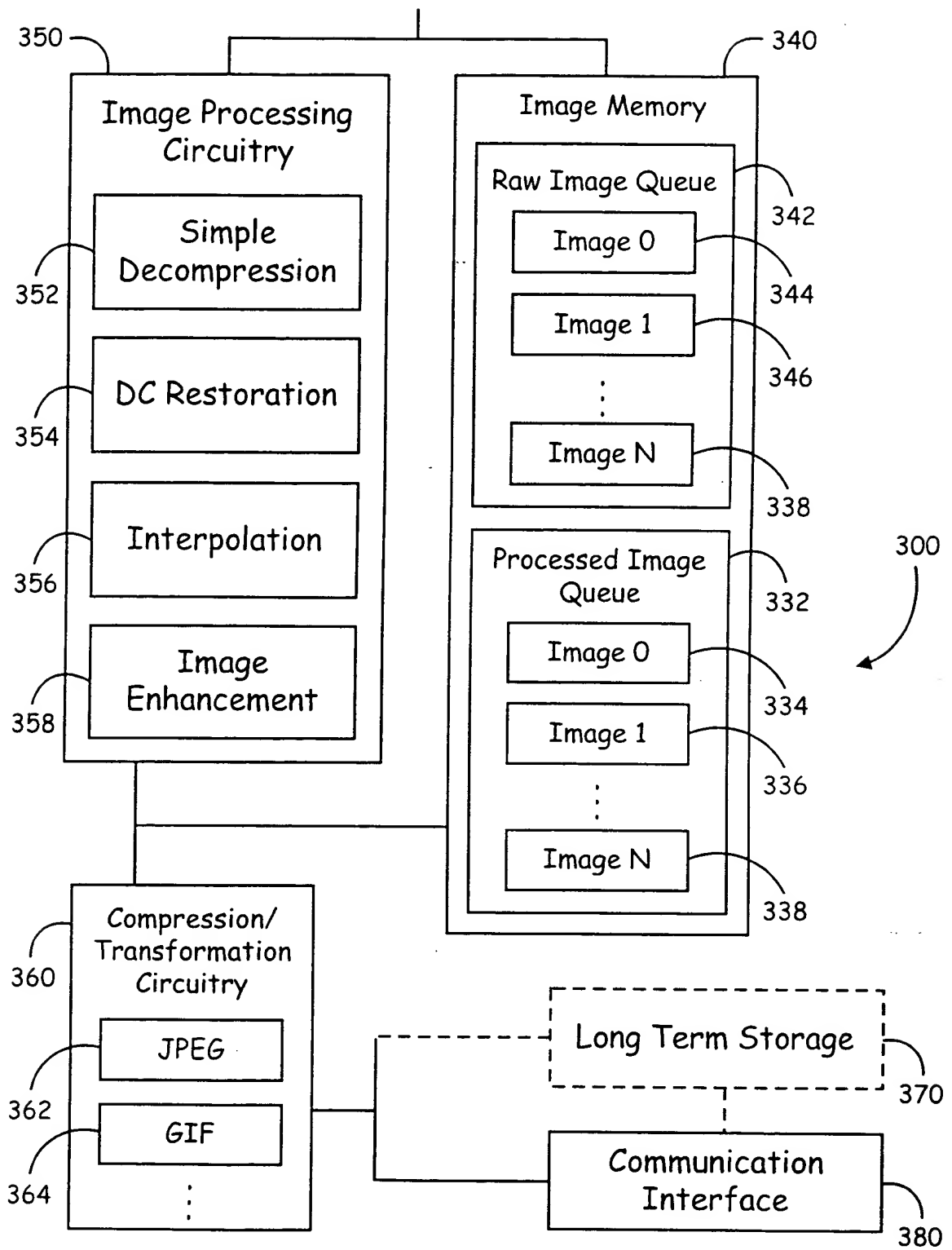


Fig. 3

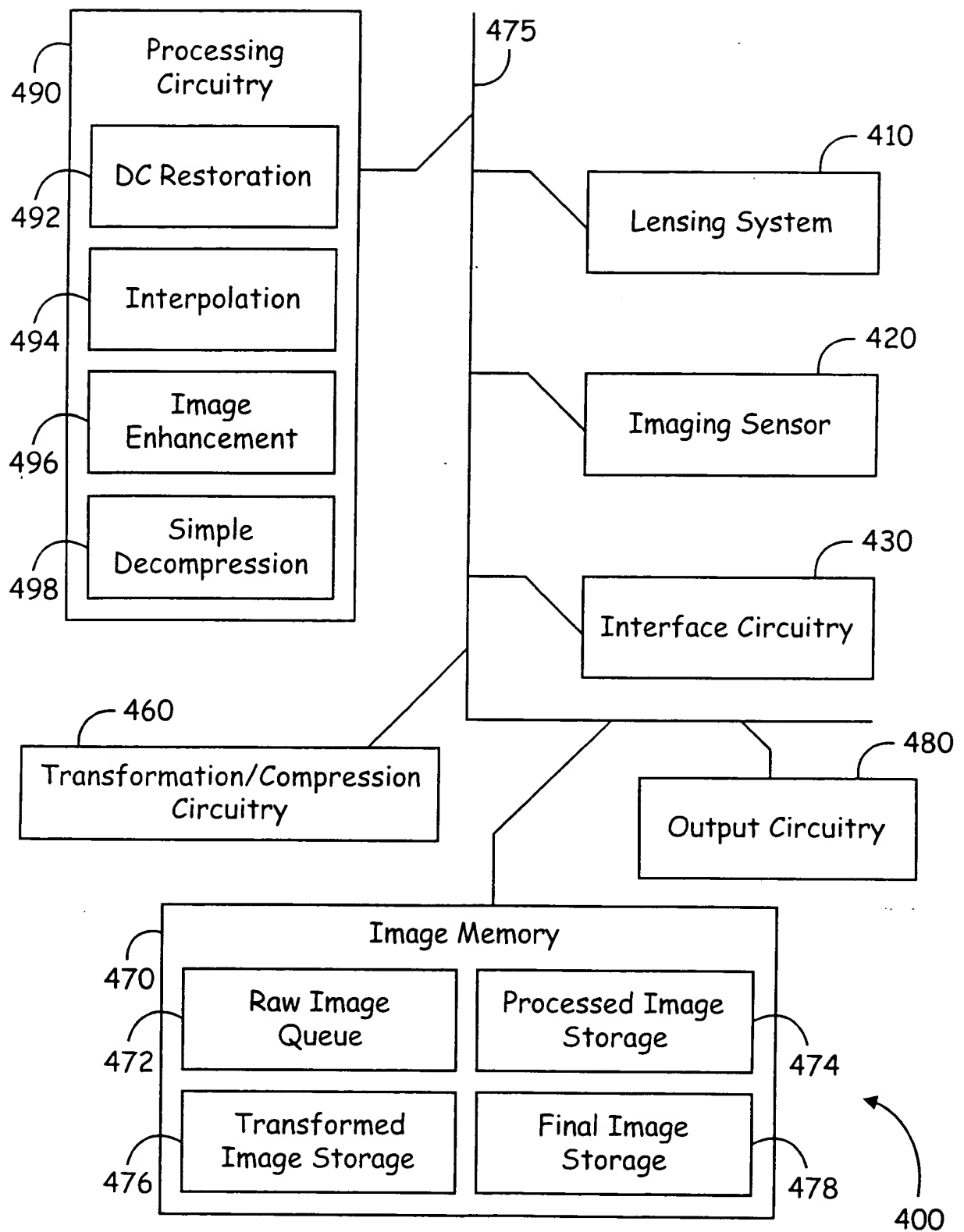


Fig. 4

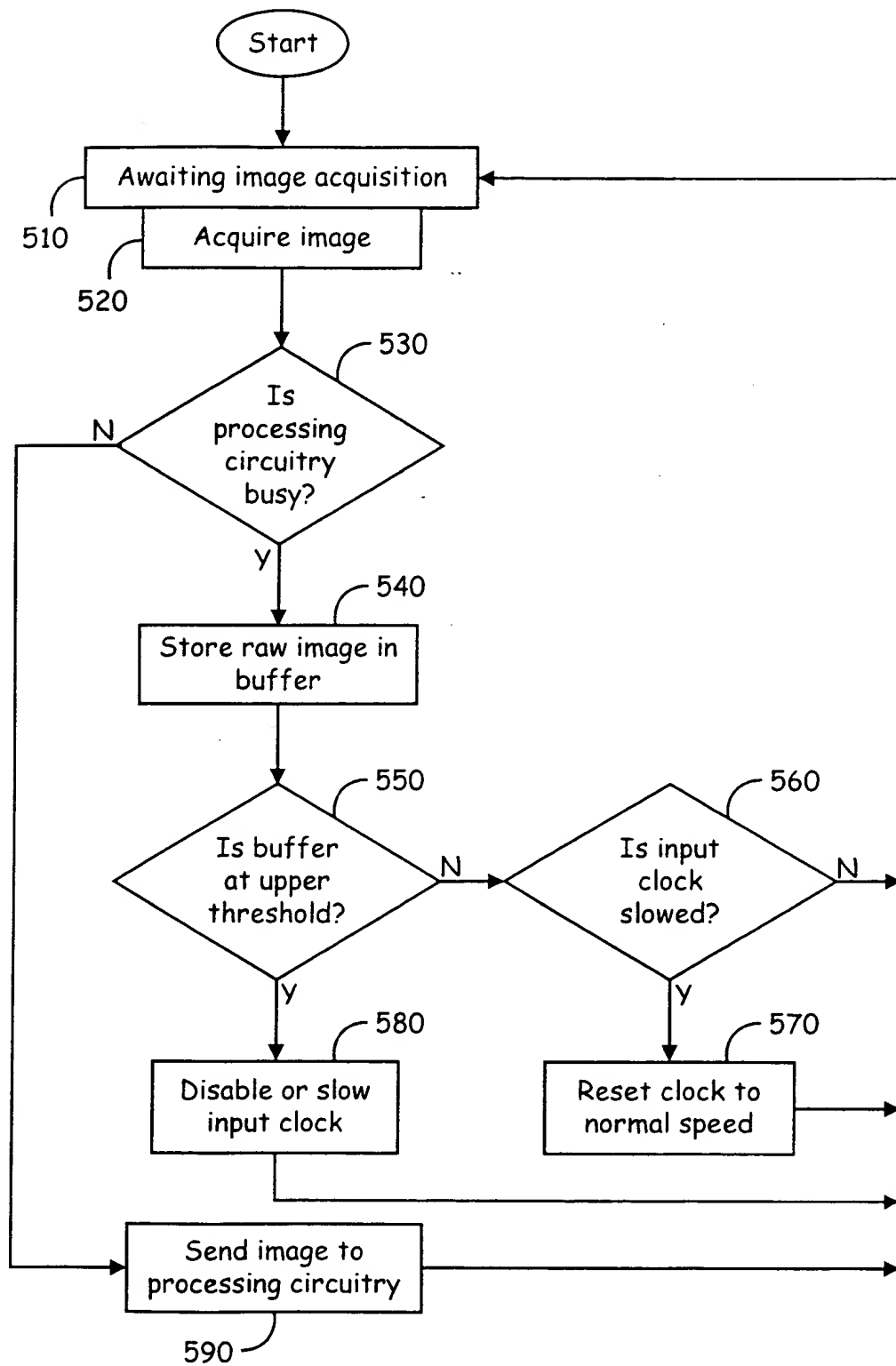


Fig. 5

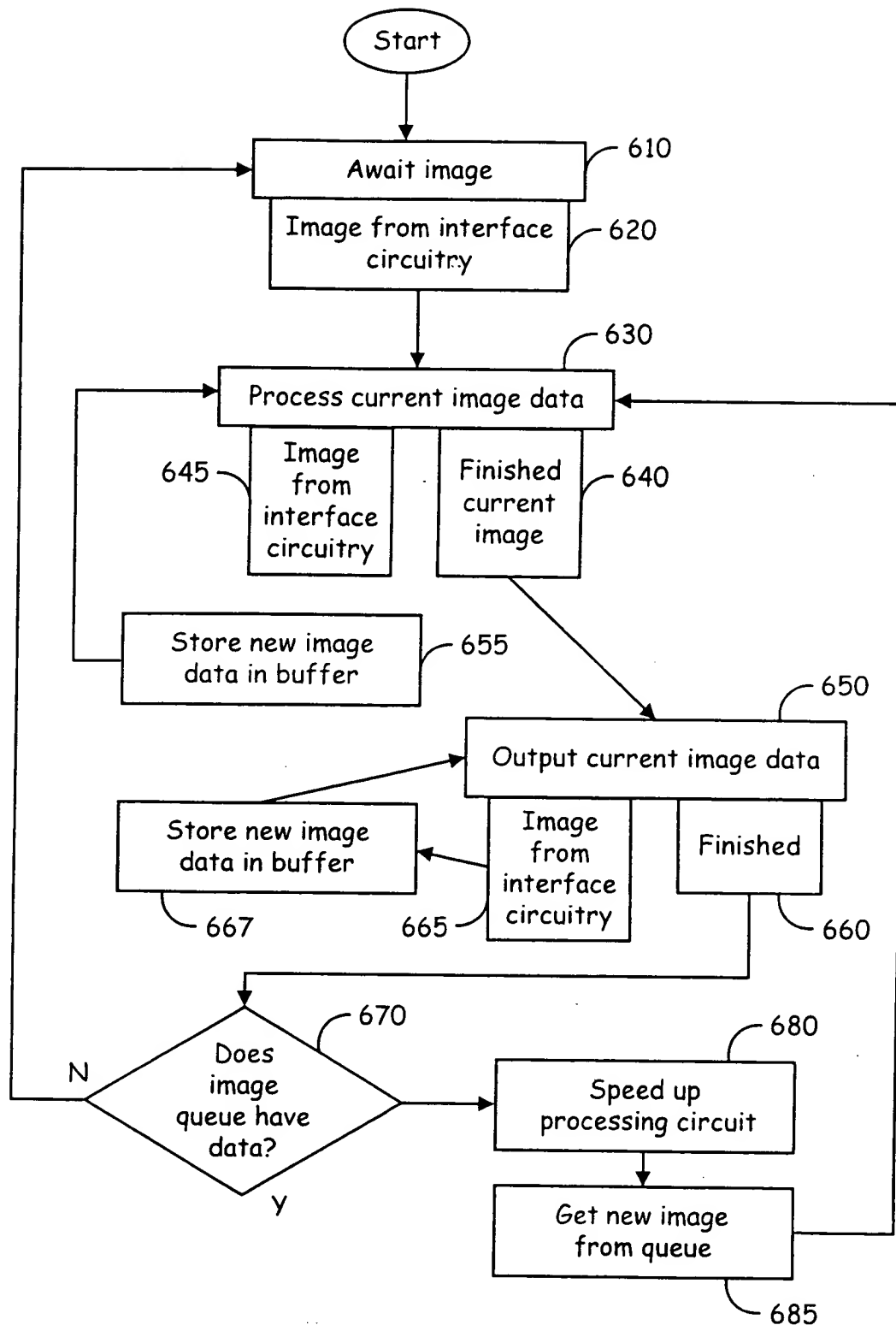


Fig. 6

FIG. 7a is a block diagram of an image processing circuitry 710. The circuitry 710 includes a plurality of processing circuitry blocks 720a, 720b, ..., 720n. Each block 720a, 720b, ..., 720n is connected to a common bus 711. The circuitry 710 is configured to process an input image and output a processed image.

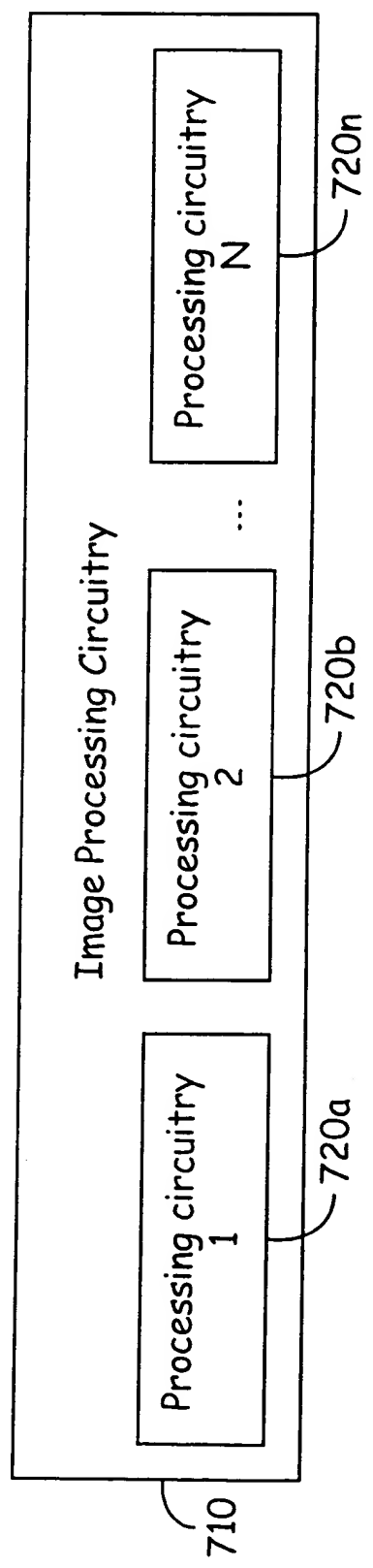


Fig. 7a

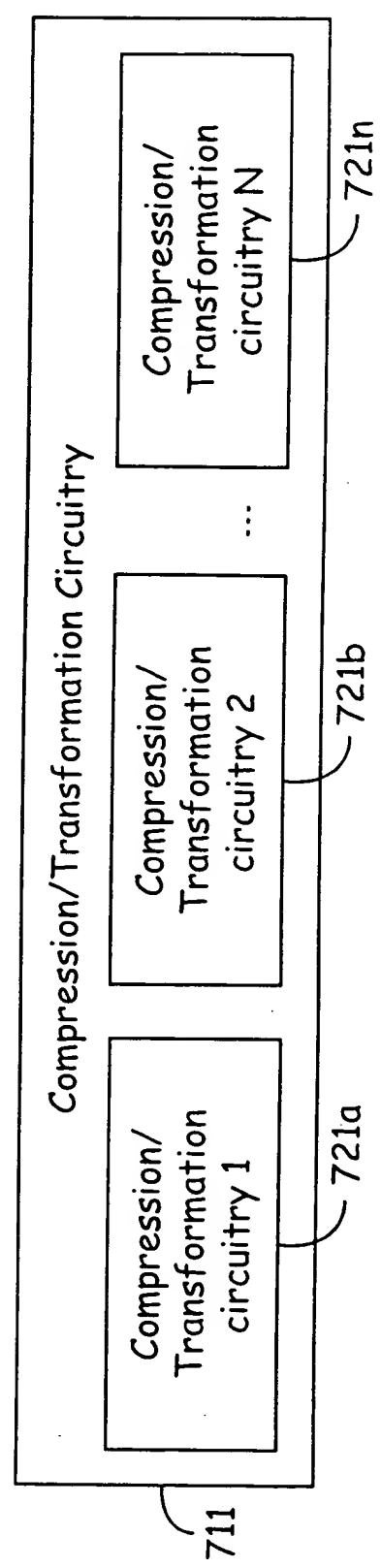


Fig. 7b

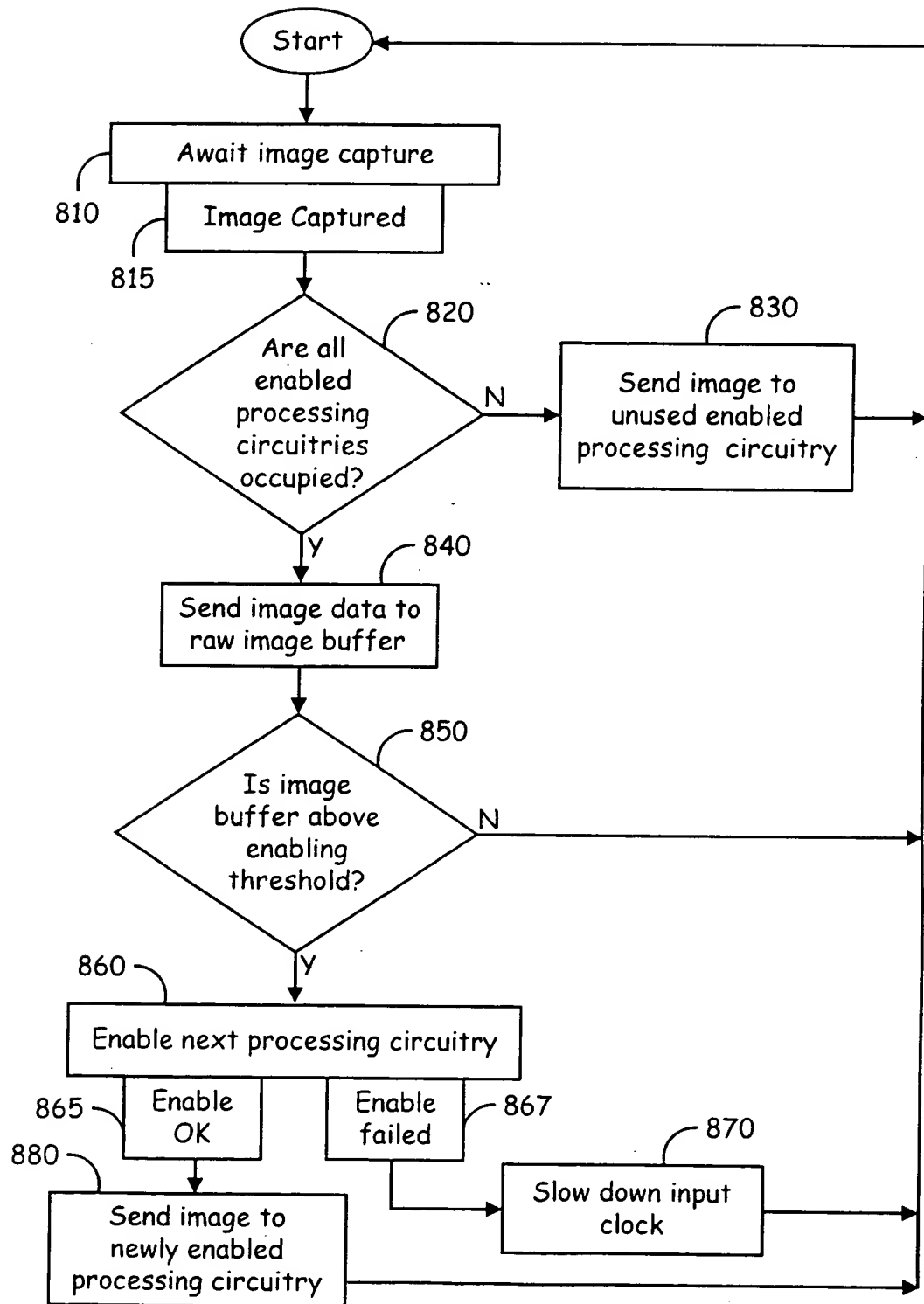


Fig. 8



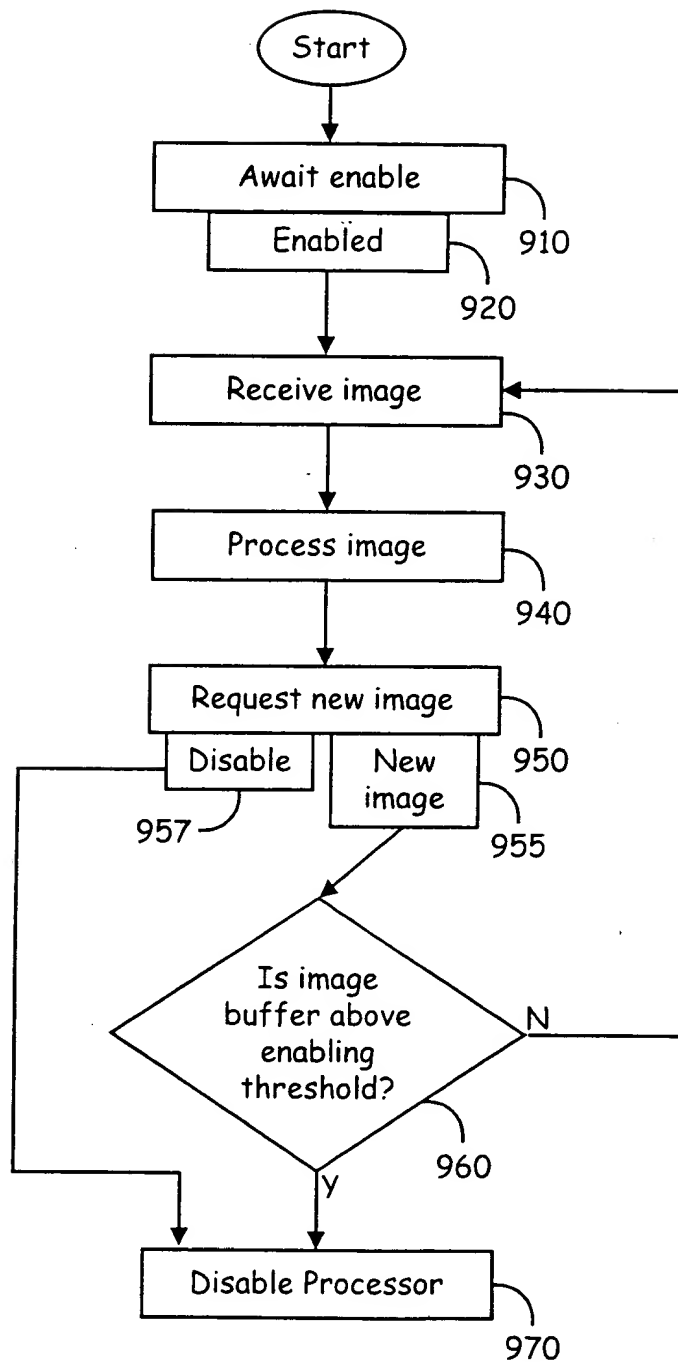


Fig. 9

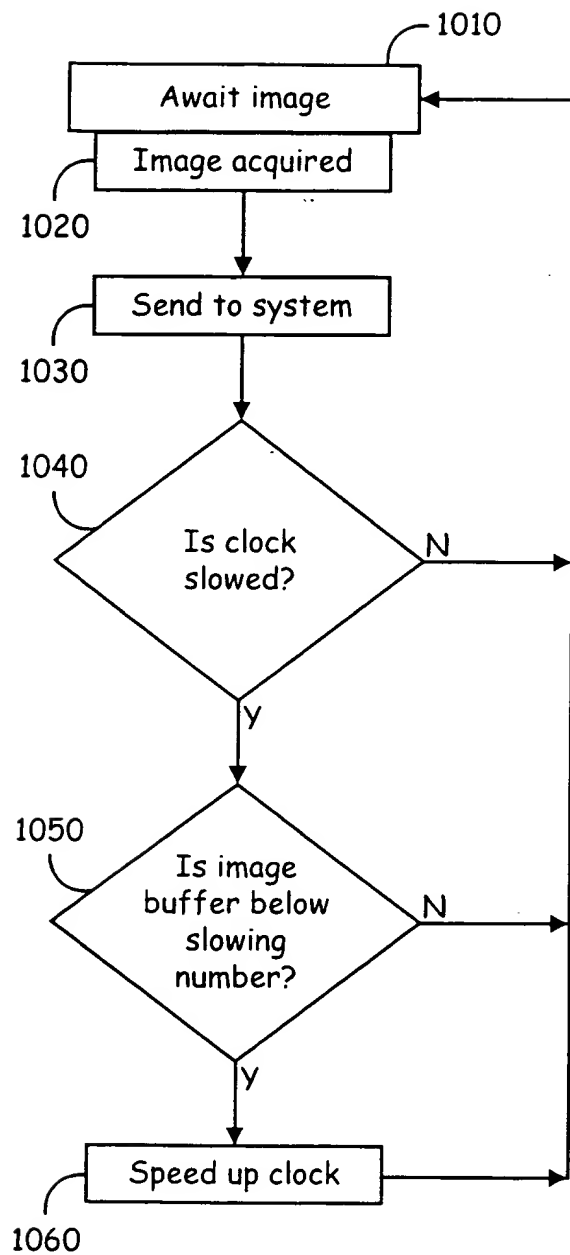


Fig. 10

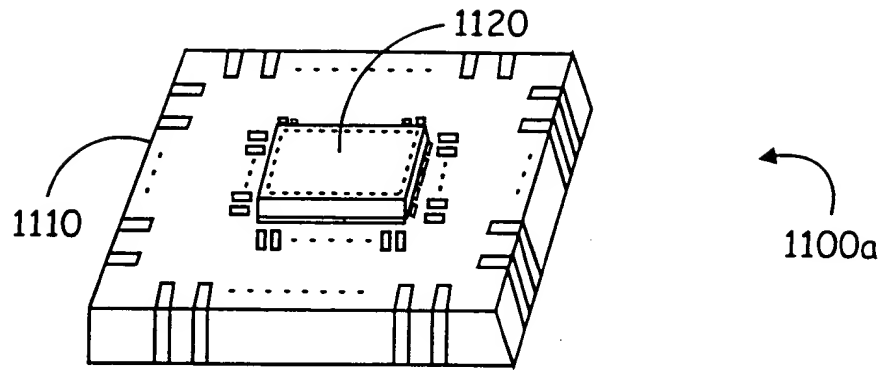


Fig. 11a

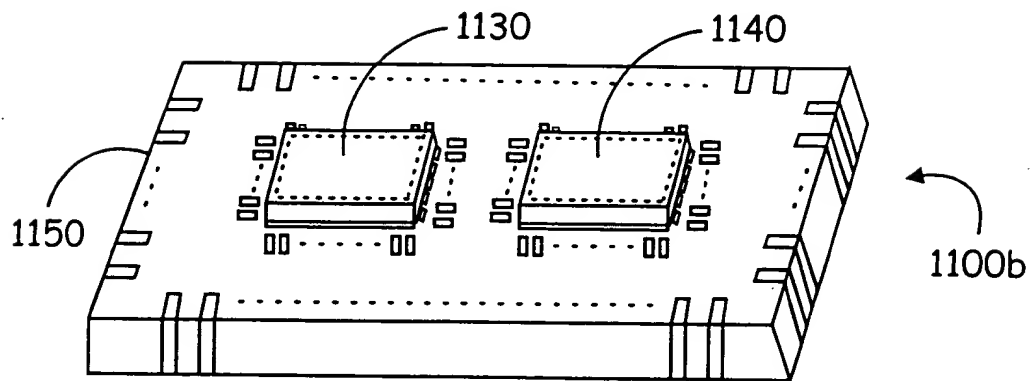


Fig. 11b